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An Advanced Direct-Digital VFO

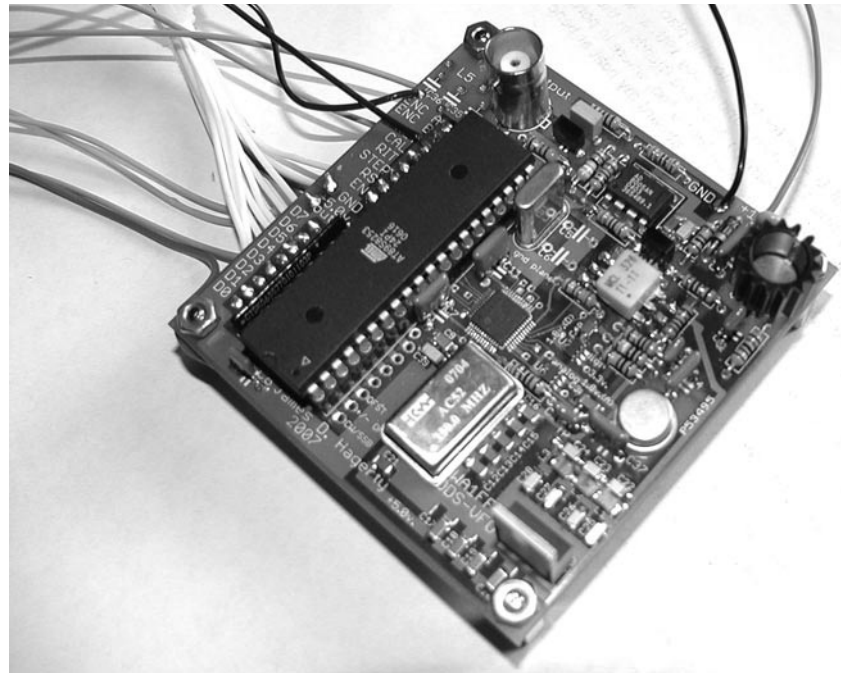
The author used an Analog Devices AD9951 DDS IC in a new VFO design.

A number of radio amateurs, including the author, have built direct digital VFOs with the Analog Devices AD9835 and the AD9851.[1] Although powerful software features have been available for these projects, there was a significant limitation in the hardware: the 10-bit D/A converter at the output limits the spurious-free dynamic range (SFDR) to about 60 dB. This is a critical parameter if such a device is used as a local oscillator, because even very low-level spurs can mix with weak adjacent signals, severely compromising dynamic range.

This article describes a hardware design that features the Analog Devices AD9951.

A 14-bit D/A converter at the output, and a much higher rated clock speed than the 98xx family allows a frequency-dependent SFDR in excess of 70 dB, and approaching 80 dB with a 400 MHz internal clock frequency. It puts the latest technology on a four layer, 3 inch circuit board, and can be used as a stand-alone VFO or as part of a multi-loop frequency synthesizer. There are two stages of RF filtering included in the design: the first between the 9951 DDS and the output buffer amplifier, and the second after the buffer, at the board output. A significant capability for software expansion exists, as only about 2 KB of program memory (out of an available 12 KB) is presently used. As in previous designs, tuning is accomplished with a shaft encoder. An inexpensive LCD provides a frequency readout.

Present software features include a calibration routine to null out clock frequency error, RIT (receive incremental tuning) spanning ± 10 kHz, an improved method for changing the tuning step size, and flash EEPROM storage of all RAM data. This last feature allows the most recent calibrated carrier to come back up after power down. Additional new software features are under development. The oscillator is tunable over the entire HF band. Higher output frequencies are possible if the clock frequency is increased. The complete design, software, and board were developed using tools costing the equivalent of an entry-level transceiver.



The AD9951 DDS IC was chosen as the successor to older DDS IC families because of its greatly improved spectral purity, its suitability as a local oscillator and its powerful architecture. For example, one of the many new features of this chip is a programmable rise-time parameter to minimize side lobes, such as those causing key clicks. All of these features come at a price of significantly greater complexity. The chip is contained in a 48-pin surface-mount package about the size of a small fingernail. A special surface-mount template was made for this part using the printed-circuit layout package, *Eagle*. Tom Riley, a friend and an expert with *Eagle*, helped me with this. Fortunately, it fit perfectly the first time.

Three supply voltages are required for the 9951: 1.8 V analog, 1.8 V digital, and 3.3 V for the interface pin. The chip runs on a 1.8 V core, a startling difference from the "old" 5 V logic many are used to. The 9951 can be directly interfaced with 5 V logic once the 3.3 V is supplied on pin 43. Analog Devices engineers have told me that the much greater chip circuit density mandates these lower supply voltages. The technology is impressive: at present I am clocking this chip with its 1.8 V core at 150 MHz. Several programmable internal clock multiplier factors are available to increase this up to the rated value of 400 MHz.

Circuit Design Architecture

Figure 1 shows the complete circuit of the direct-digital VFO. The overall intent of this project was to put the most advanced hardware on a compact board immediately and concentrate on elaborate software features later. Still, there were several features that I wanted, and these were given high priority.

[1]Notes appear on page 24.

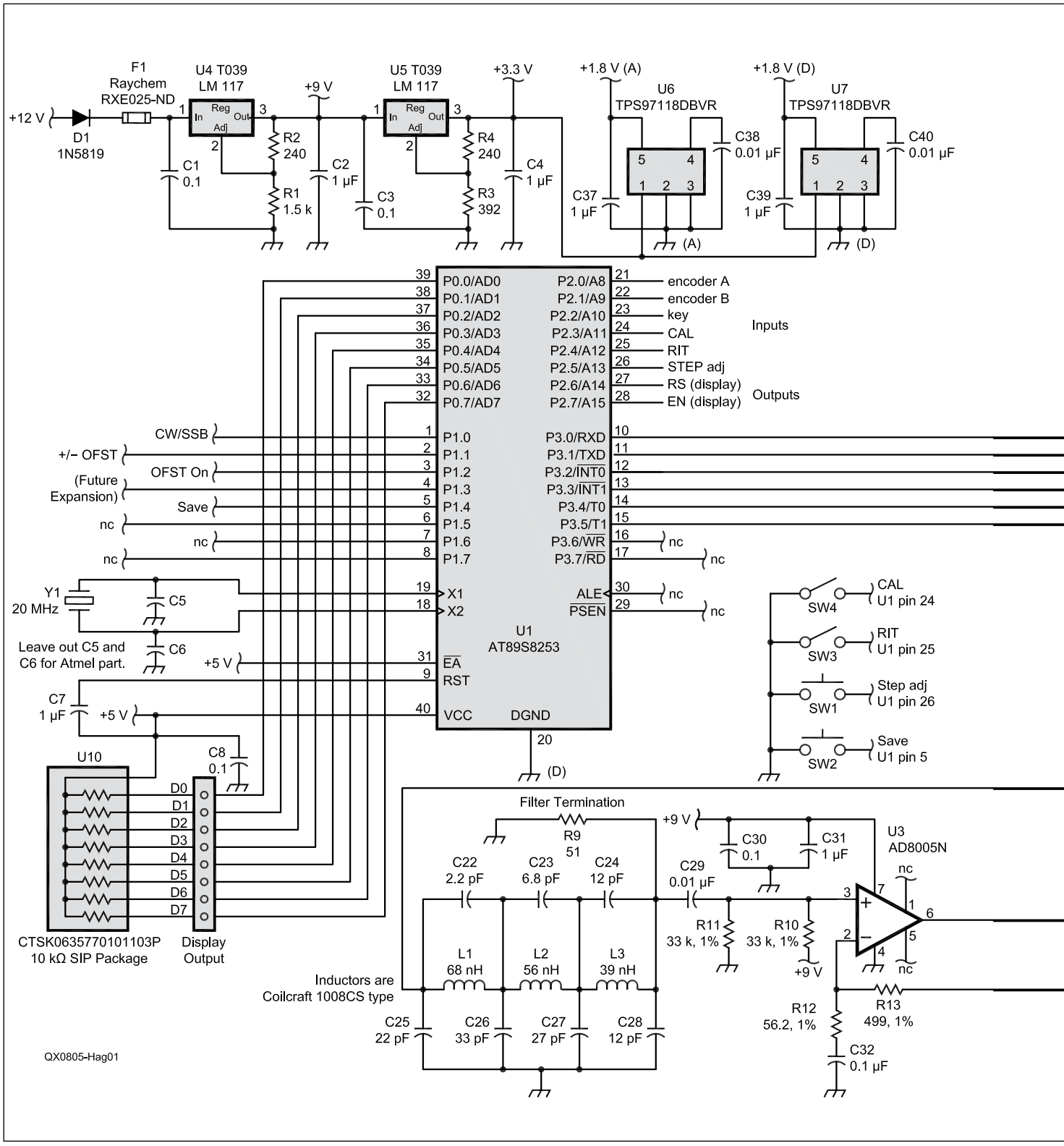
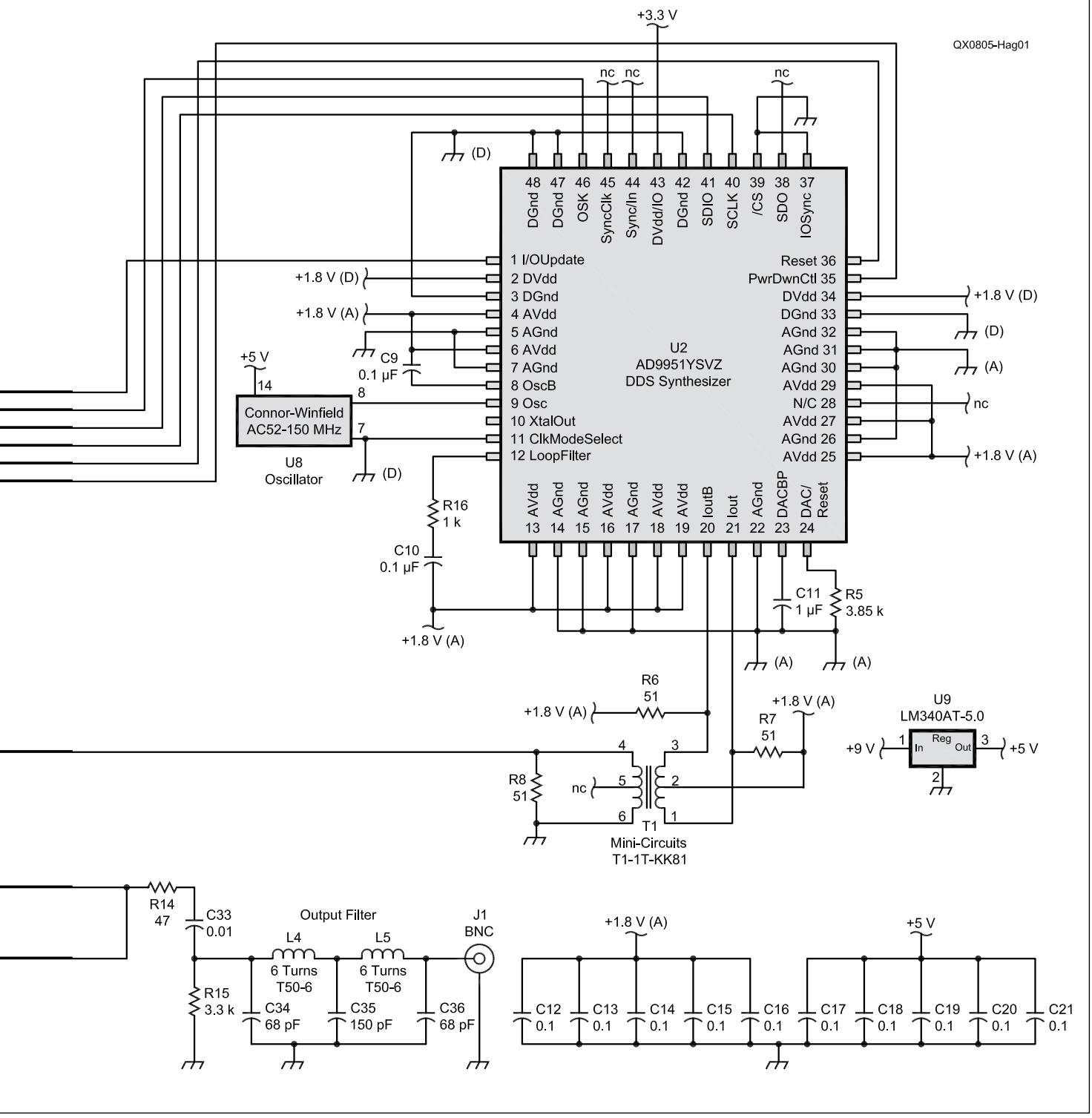


Figure 1 — The schematic diagram for the direct digital VFO uses an AD9951 DDS IC, and an AT89S8253 microprocessor.



The multiple supply voltages required by the 9951 provided new challenges for the board layout. Analog Devices recommends a 4-layer board for this part. The top layer is the surface-mount layer, followed by a ground plane layer, power plane, and a final ground plane at the bottom. In addition to the two 1.8 V supplies and the 3.3 V interfacing voltage, a 9-V regulator was added to power the output buffer stage. This was a single-supply RF op amp (AD8005) similar to that in the 2002 article. The 1.8 V supplies, which were only necessary for the AD9951, were provided by small surface-mount, fixed-voltage regulators made by Texas Instruments.

The 3.3 and 9 V regulators were implemented with the well-known, adjustable National LM117 metal-can devices. The metal-can packaging was chosen to provide ease of heat sinking. Finally, a 5 V regulator was added to power the microprocessor, LCD display, and the shaft encoder, as my search for 3.3 V displays and shaft encoders had turned up very little.

The microprocessor used here is a recent offering by Atmel that incorporates the common 8051 instruction set. I had experience with this language and developed the assembly language software first by using an assembler from American Automation (no longer supported) and then a more recent one by Metalink. The chief attraction of the Atmel part was the 2 KB of flash EEPROM, giving the designer great expansion capability to store frequencies, implement memory stacks, and so on. The part was programmed with a Needham Electronics EMP-21. This is a new, USB-driven product. The Atmel part has a rated clock speed of 24 MHz. Faster 8051 parts such as those by Philips are available with up to 33 MHz clock ratings but without the flash EEPROM.

In the early stages of the design, I debated the use of separate clock oscillators for the microprocessor and DDS. The Atmel part is designed to operate without capacitive loading on the crystals, making it extremely attractive for a compact board. The 9951 has a feature allowing it to be driven by a significantly lower frequency clock (at U8) with the internal phase-locked loop multiplying up the actual internal clock frequency. For flexibility I chose to clock the microprocessor and DDS with separate oscillators. The spectral plots of the results have been reassuring, and stability measurements indicate only the small drift of the clock oscillator specifications, such as 50 ppm or 100 ppm. Clocking the DDS with, say, a TCXO (temperature-compensated crystal oscillator) will give even greater stability. Analog Devices states that the quality of the DDS output in terms of phase noise is directly related to the quality of the DDS clock oscillator. The one presently used is a Connor-Winfield AC52 and it clocks the DDS directly (DDS internal clock multiplier disabled) at 150 MHz. It was obtained as a development sample. The microprocessor is driven by a 20 MHz crystal.

For the best spectral purity possible there are two stages of filtering included on the circuit board. The first, a 160-MHz low-pass filter just after the transformer-coupled output from the 9951, was taken directly from the 9951 evaluation board. Analog Devices uses the transformer T1 on its evaluation board (EVB), and recommends it for the best performance. Although this small transformer (made by Mini-Circuits) is meant for surface-mount construction, I was able to solder it carefully to the board without too much trouble. The first low-pass filter uses surface-mount inductors made by Coilcraft. These were obtained as samples. The capacitor values were readily available. As I prototyped the board, I found it helpful to standardize all surface-mount parts to the "1206" size, which is large enough for practical handling but still offers a wide range of component values.

The second stage of filtering is at the very output, and is a classic two-stage low pass filter. Values were taken for a cutoff of slightly greater than 30 MHz. Other design values are in the article, "A Progressive Receiver," by Wes Hayward and John Lawson.[2]

Layout and Construction

After choosing the AD9951 for the new board, I purchased the software layout program *Eagle* (standard version), and used that to put together a layout. Although much is made of using large ground planes, I have always felt that they are not a substitute for a good layout. Much time was spent in orienting the parts to give the shortest possible lead lengths and the most direct ground return paths. Then the ground and power planes were put into the layout. Care must be taken not to "stitch" ground and power planes together with through holes when changes are made. *Eagle* automatically generates good-quality Gerber files and can be used to design a complete product. The cost of this software package was about $200.00. A library of surface-mount parts is included, as well as a component editor. As mentioned before, the AD9951 template, as well as that for the transformer, were custom made for this application.

Samples were obtained for the AD9951. There is a small square of metal on the bottom side of the 9951 package, which must be soldered to ground for best low-noise operation. This is incorporated into the assembly process. A local surface-mount assembly technician was enlisted for a small fee to hand-solder the surface-mount parts onto the prototype board. While the AD9951 and TI 79118 regulators had multiple, closely spaced leads and required the use of a professional assembler, I believe that the rest of the surface-mount parts (many of which are simply filter capacitors) could be easily soldered by hand. Tom Riley — a friend mentioned earlier — does much of this assembly using

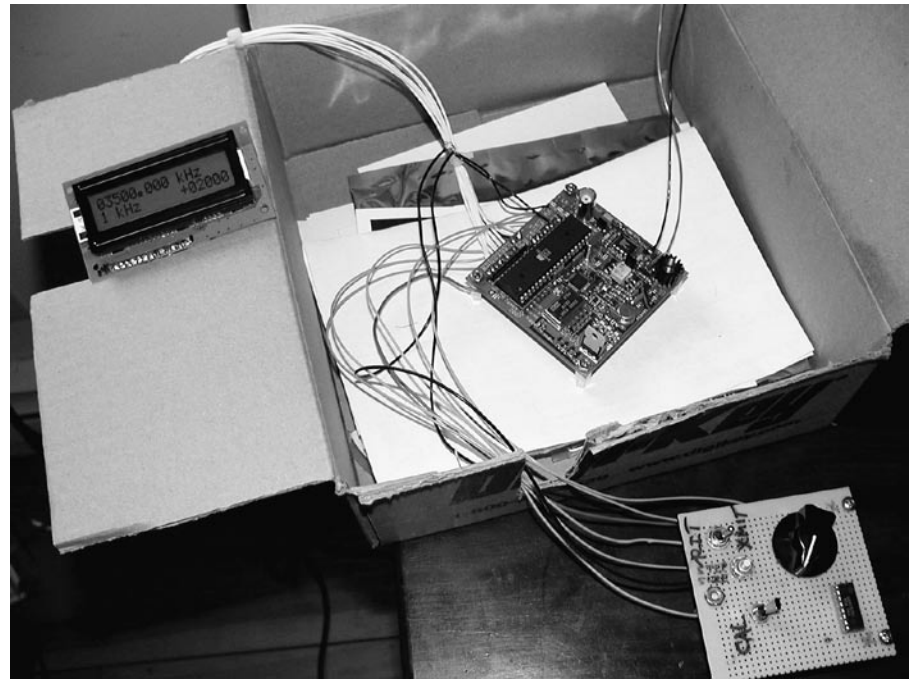


Photo B — This "Box Board" prototype shows the main DDS circuit board, LCD circuit board and the input controls wired on a piece of perf board.

tweezers and silver epoxy with good results. The larger, 1206-sized surface-mount parts make this even more possible. Through-hole parts were used whenever possible, but the 160 MHz filter was implemented with surface mount construction in order to duplicate the Analog Devices evaluation board as much as possible. Circuit boards and partial kits for the DDS VFO are available. Check the author's Web site at **www.WA1FFL.com** for the latest updates, kit options and information, and application notes for the VFO.

Prototyping has changed radically in the past twenty years, with designers often being forced to go right to a circuit board layout in order to get surface-mount components working. It has become a fact of life. Many components in the RF world are only available now in surface-mount packages. A noteworthy article by Walt Kester of Analog Devices discusses the difference in RF characteristics between a through-hole-packaged RF op amp (the AD8001) and its surface-mount equivalent.[3] Surface-mount filter capacitors are generally preferred as they have smaller lead inductance.

Testing and Results

After the board was constructed, measurements were made before connecting the display and shaft encoder. The supply voltages came up correctly the first time. Despite some minor cosmetic issues, all electrical connections were as desired. Attention was then diverted back to software development, in particular, getting the microprocessor to generate the correct control signals to download the AD9951 with the correct frequency. This was done with simple subroutines after extensively studying the 9951 control registers bit-by-bit in the data sheet. After some brief debugging, a clean 21 MHz carrier was generated at the board output. The 21 MHz output was significantly better in quality than the 10 MHz waveform on the previous VFO design. Because of the very low supply voltages on the AD9951, one must expect a much lower output voltage at the chip — on the order of 100 to 200 mV.

The spectral plots in the 9951 data sheet begin at –4 dBm, a level of only 140 mV across 50 Ω. With the output buffer in place, the board's unterminated output was about 1 V peak across most of the HF band. A 50 Ω termination on the output filter is expected for correct performance. To boost the output level even more, an external buffer amplifier may be used to supplement the VFO output stage. One that is highly recommended was described by Doug DeMaw, W1FB, in a QST article.[4] It includes another stage of output filtering and uses a 2N5179 transistor. It was originally designed by Wes Hayward, W7ZOI.

Work proceeded on the display and shaft encoder wiring, which came up immediately. A new model of shaft encoder, the Grayhill 61K64, was used. The 61K25, which has a much slower tuning rate, was preferred and obtained as a sample, but was difficult to find in stock. Another model by CUI with an even slower tuning rate (20 pulses per revolution) is being evaluated as well. It has smooth detent operation and is well-made and affordable. The VFO software was modified to allow the shaft encoder to operate as a tuning step size selection device, while a momentary push button switch is held down. While holding down the push button, the shaft encoder is rotated until the desired tun-

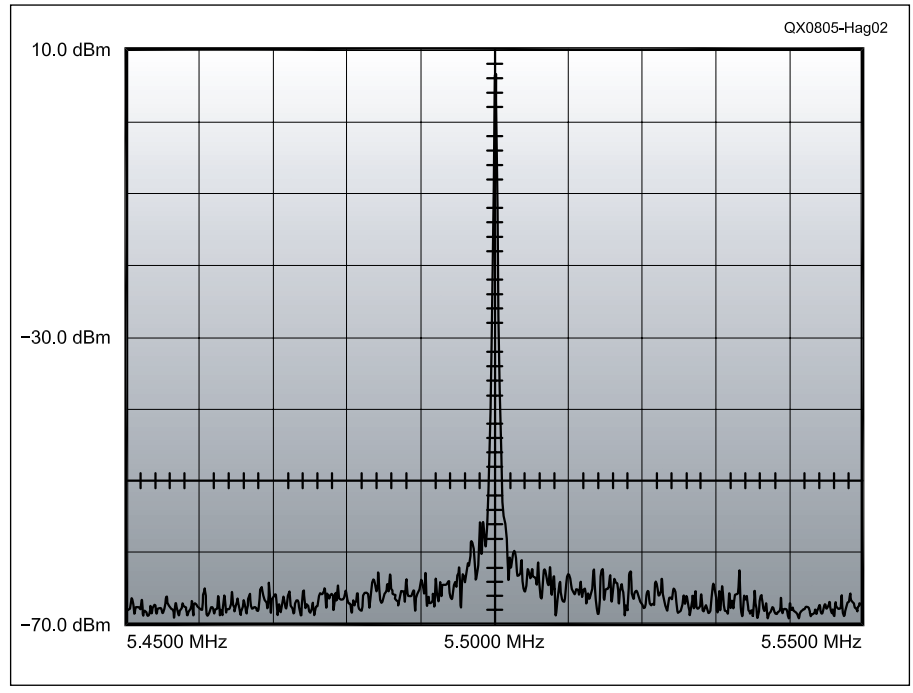


Figure 2 — This spectral output display shows the VFO operating at 5.5000 MHz. The top of the display represents 10 dBm. The input signal has been attenuated by 40 dB.

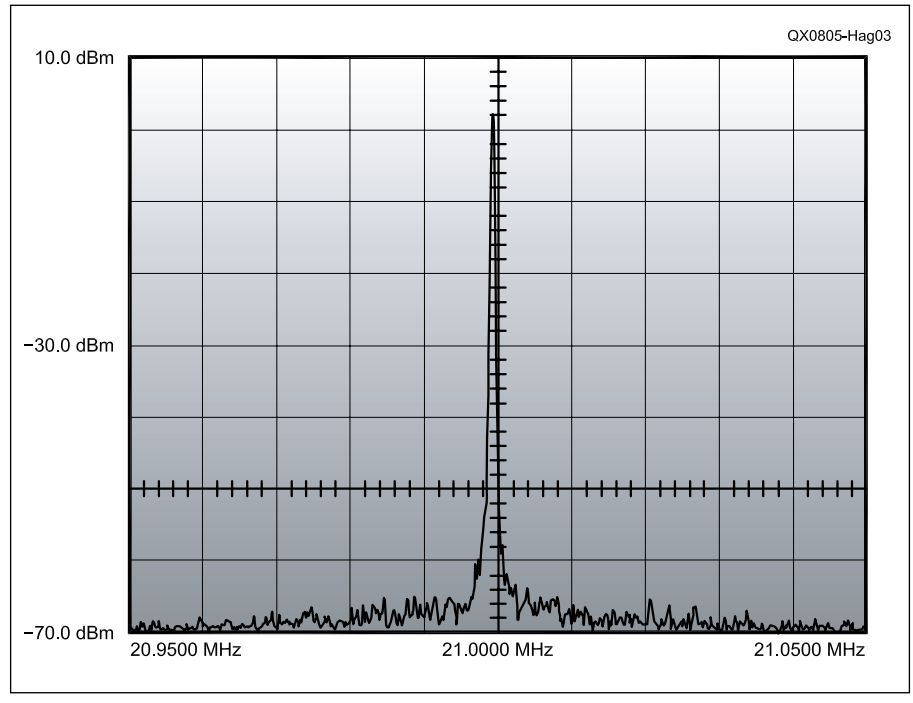


Figure 3 — This spectral output display shows the VFO operating at 21.0000 MHz. The top of the display represents 10 dBm. The input signal has been attenuated by 40 dB.

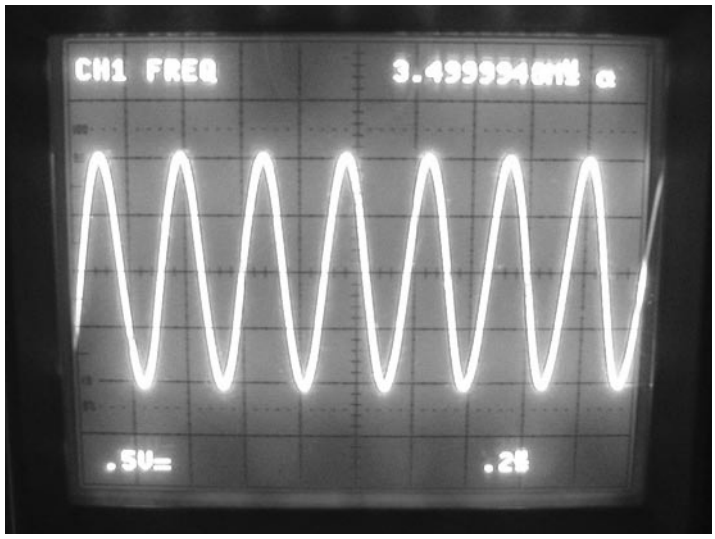


Photo C — This clean sine wave output is with the DDS VFO operating at 3.499994 MHz.

ing step is selected. Step sizes of 1 Hz up to 1 MHz are available with this design. A version of this feature using a rotary switch was also successfully implemented but put aside due to the cost and size of the switch.

The display is a standard 16 × 2 LCD with equivalent versions made by Optrex, Varitronix, and other companies. To minimize power consumption, a back-light is not used.

A software calibration feature was implemented to null out clock frequency error. Throwing the CAL switch freezes the display and allows the operator to add or subtract 1 Hz. steps until the carrier is "spot on." Then, the calibrated carrier is saved in flash EEPROM by pressing the SAVE switch. This feature thus acts like a trimmer capacitor that is implemented in software.

Another feature that was desired was receive incremental tuning (RIT) and this was programmed to appear in the lower-right corner of the display. An offset of plus or minus 10 kHz is available. The RIT display reads directly in Hz. The RIT is tuned in 10 Hz steps until the desired offset is achieved. Throwing the RIT switch back to the off position restores the carrier to its former value. Another option would be to program a separate VFO display on the bottom ("B side"). I concluded that this would be easier to program than the separate RIT because of its inherent symmetry, and have added this option to my wish list.

Most importantly, spectrum measurements were made on several example waveforms.

See Figures 2 and 3. Because of the popularity of 5.0-5.5 MHz as a local oscillator tuning range, it was desired to focus somewhat on this region. Measurements at 5.5 MHz showed a spurious-free dynamic range of about 72 dB. This could be increased with a higher clock rate (up to 400 MHz.) More measurements will be made accordingly. At 21 MHz, the SFDR was about 70 dB.

The next step will be to program in a clock multiplier of 4× for an internal DDS clock frequency of 400 MHz and perform the same measurements. This implies the use of a 100 MHz clock oscillator on the board. Other clocking methods will produce different results. The spectral plots in general, which were the very first made on this board, mirrored the narrow-band results given in the data sheet very well. More experimentation and evaluation are anticipated.

In general, the purest waveform and highest SFDR will be obtained while running the VFO at the highest possible clock frequency. The output frequencies will appear cleaner. The tightest filtering possible should be used, consistent with tolerable roll-off at the highest output frequency.

Total current drain of the board using the Connor-Winfield 150 MHz oscillator, and with the display connected, was 150 mA. Using a clock oscillator by International Crystal that operated at 100 MHz, the current drain dropped to about 80 mA, but the much lower clock frequency resulted in noticeable waveform distortion at lower frequencies, as expected. Higher frequency clock oscillators using YIG devices are available but I have not evaluated them. There are many possibilities left for experimentation.

The use of the microprocessor flash EEPROM has given even more possibilities for expansion. I recently added 16 memory storage locations for frequency configurations, with expandability to 32 memories. In addition, plus or minus keying offset is now available for CW (700 Hz) and SSB (1.5 kHz).

I eagerly await the development of DDS ICs that give full 16-bit performance at the output D/A stage, for 90 dB SFDR. New design techniques and IC technology will only improve performance.[5]

Acknowledgements

I want to acknowledge the assistance of Tom Riley, who provided the surface-mount template for the AD9951. He was also helpful in advising me about surface-mount prototyping techniques. Jeremy O'Neal saved me much time by alerting me to the zero-padding requirements of the *Eagle* drill file coordinates. Paul Mileski generously gave of his time in helping me set up spectral plots. Wes Hayward, W7ZOI, gave me valuable feedback after the previous VFO article and I appreciate his rigorous approach and his comments about the necessity for spectrally-pure local oscillators and their relationship to dynamic range. Dan Duang of Atmel and David Brandon of Analog Devices gave valuable advice on device applications. Much gratitude goes to Mitchell Lee of Linear Technology Corp for his helpful suggestions.

Notes

[1]James D. Hagerty, WA1FFL, "A Compact, Direct-Digital VFO," *QST*, Jan 2002, pp 35-38.

[2]Wes Hayward, W7ZOI, and John Lawson, K5IRK, "A High-Performance Communications Receiver," *The ARRL Handbook for the Radio Amateur*, ARRL, 1985 through 1994 editions, pp 30-8 to 30-15.

[3]Walt Kester, (Analog Devices), "Prototyping Techniques Help Verify Analog-Circuit Performance," *EDN*, Feb 15, 1996, pp 131-140.

[4]Doug DeMaw, W1FB, "Accessories For Your VFO," *QST*, Jan 1988, pp 31-34.

[5]Ken Gentile, and Roger Huntley, (Analog Devices), "Signal Cancellation Improves DDS SFDR," *Microwaves and RF*, Aug 2006, pp 120-128.

References for Additional Reading

Charles Kitchin, "Avoiding Op Amp Instability Problems in Single-Supply Applications," *Analog Dialog*ue (Analog Devices), Volume 35-2 (2001), pp 12-14.

"Exploring the Synthesizer in a Commercial MF/HF Transceiver," *The ARRL Handbook for the Radio Amateur*, 1999, pp 14.49-14.51. Describes the use of DDS in the ICOM IC-765 transceiver, as part of a multiloop synthesizer. Here, the DDS subsystem is operated at very low radio frequencies for the cleanest spectral performance possible.

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James D. Hagerty, WA1FFL, is an electrical engineer in Newport, RI. He has been licensed since 1965. Jim is an EE graduate of Cornell University and holds an MSEE from the University of RI. He holds 10 patents. QEX